

REMARKS

Claims 1 – 10 are pending in the application.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 1 - 10 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2002/01100086 to Reches. Applicants respectfully traverse this rejection.

In independent claim 1, Applicants disclose a packet switch including: a) N input buffer sections, provided for respective N input lines, for storing unicast packets and multicast packets input through corresponding input lines, b) a switch section for outputting a unicast packet to any of M output lines to which the unicast packet is transmitted when the unicast packet is input from each of the N input buffer sections, and outputting the multicast packet to a plurality of M output lines to which the multicast packet is to be transmitted when the multicast packet is input, and c) a scheduler section for selecting the unicast packet or the multicast packet to be output from each of said N input buffers such that the input lines and the output lines cannot conflict each other for the unicast packet, and such that the input lines cannot conflict each other for the multicast packet.

Reches discloses a multiport switch for forwarding variable length packets, including packets of unicast and multicast types (see, e.g., abstract and paragraph [0036] of Reches). The switch of Reches includes a plurality of buffers each for storing different packet types, a switch for outputting packets to a plurality of output lines or ports, and a scheduler for scheduling packet transmissions to avoid conflicts (see, e.g. FIG. 1, paragraphs [0061] to [0067]). However,

unlike Applicants' claimed invention, the switch of Reches does not disclose or suggest distinct scheduling processes for each of unicast and multicast packets.

As claimed for example in Applicants' claim 1, the scheduling section schedules "the unicast packet or the multicast packet to be output from each of said N input buffers such that the input lines and the output lines cannot conflict each other for the unicast packet, and such that the input lines cannot conflict each other for the multicast packet. In other words, in a given scheduling cycle, the scheduling section operates to select only one packet from each input line, and in the case of unicast packets, additionally selects only one packet from one input line for a given output line in the cycle (see, e.g., page 16, line 25 through page 19, line 23 of Applicants' specification, with reference to Applicants' FIGs. 7A – 7D and 8). Unlike Applicants' claimed invention, Reches neither discloses nor suggests a scheduling process that distinguishes selection rules as to unicast and multicast packets. Accordingly, Applicants respectfully submit that claim 1 is not anticipated by Reches, and is therefore allowable.

As claims 2 – 10 depend from allowable claim 1, Applicant submits that claims 2 – 10 are allowable for at least this reason.

CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that claims 1 – 10, consisting of independent claim 1, and the claims dependent therefrom, are in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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